## REMARKS

**CLAIMS:**

Claims 1-49 comprise the case.

**I) Typographical Errors:**

A) Applicants have amended Claims 2 and 10 to correct a typographical error, correcting "closet" to "closest".

B) Applicants have amended Claim 33 to correct a typographical error, correcting the claim to depend from Claim 30 instead of Claim 27.

Applicants respectfully submit that no new matter has been added in any of the corrections.

**II) 35 U.S.C. 102, Claims 1-38:**

Claims 1-38 are rejected under 35 U.S.C. 102(b) as being anticipated by Jardine et al. (USPN 5,884,018).

A) Claims 1, 10, 20 and 30:

With respect to Claims 1, 10, 20 and 30, the Examiner states that Jardine discloses a "plurality of processor nodes each independently testing access to at least one other of said processor nodes on said multi-drop network; upon *** detecting a failure to access at least one of said other said processor nodes, said failure detecting processor node determining, from said information of relative locations, the processor node having failed access which is closest to said failure detecting

processor node; and said failure detecting processor node storing an identification of said closest processor node having failed access ***".

As pointed out by the accompanying Declaration under Rule 1.132, Jardine "describes monitoring communication among processors in a multi-path network, and which attempts to regroup in the event of a processor communication failure, e.g. 'an apparatus and protocol to determine the group of processors that will survive communications faults and/or timed-event failures in a multiprocessor system.' ***

"Jardine employs data structures, such as a matrix, that track the connectivity between the processors of the group in the multi-path network currently available to a processor.

"Location or relative locations of the processors form no part of that matrix, and location or relative locations of the processors to which there is or is not communication is not even intimated. For example, Jardine states 'The size of the connectivity matrix C is NxN, where N is the number of processors #_112 in the multi-processor system. In one embodiment, each entry in the matrix is a bit, and each processor #_112 is uniquely numbered between 1 and N. An entry C(i,j) indicates the ability of processor i to receive a message from processor j.' ***.

"The discussion by Jardine of the processing of the matrix C at column 19, lines 21-63, makes clear that no location or relative location information is involved in the matrix of Jardine.

"The discussion by Jardine of the network characteristics at column 13, lines 8-13, makes clear that no location or relative location information would be of use in tracking the network. Unlike a multi-drop bus network for which the present '705 Application determines failures, the network of Jardine has

instead 'at least two paths between every pair of processors' *** making location or relative location of no use."

Hence, Applicants respectfully submit that, without location or relative location information with respect to a multi-drop network, Jardine is unable to determine the "closest processor node", and has no interest in doing so, thereby teaching away from Applicants' invention. Therefore, Applicants' Claims 1, 10, 20 and 30 are submitted to patentably define over Jardine. For example, Claim 1 recites "In a distributed processing system comprising processor nodes coupled by a multi-drop bus network, a method for isolating failures, comprising the steps of:

"at least a plurality of said processor nodes each having information of relative locations of said processor nodes on said multi-drop bus network;

"said plurality of processor nodes each independently testing access to at least one other of said processor nodes on said multi-drop bus network;

"upon said access testing by any of said plurality of testing processor nodes detecting a failure to access at least one of said other said processor nodes, said failure detecting processor node determining, from said information of relative locations, the processor node having failed access which is closest to said failure detecting processor node; and

"said failure detecting processor node storing an identification of said closest processor node having failed access." (Emphasis added).

Applicants therefore respectfully submit that Applicants' Claims 1, 10, 20 and 30 patentably define over Jardine under 35 U.S.C. 102(b), and respectfully request allowance thereover.

B) Claims 2, 11, 21 and 31:

The Examiner states that Jardine discloses posting an identifier of the closest processor node "having failed access at an associated error indicator local to said failure detecting processor node ***".

Applicants respectfully submit that, as discussed above, Jardine is unable to determine the closest processor node, and has no interest in doing so, thereby teaching away from Applicants' invention. Hence, Applicants respectfully submit that Claims 2, 11, 21 and 31 patentably define over Jardine. For example, Claim 2 recites "posting an identifier of said closest processor node having failed access at an associated error indicator local to said failure detecting processor node." (Emphasis added). Applicants therefore respectfully submit that Applicants' Claims 2, 11, 21 and 31 patentably define over Jardine under 35 U.S.C. 102(b), and respectfully request allowance thereover.

C) Claims 3, 12, 22 and 32:

The Examiner states that Jardine "discloses upon said access testing by any of said plurality of testing processor nodes detecting a failure to access all of said other processor nodes, said failure detecting processor node posting a special identifier *** in column 22, lines 52-56."

However, Jardine is actually discussing "that no packets are getting through an any of the redundant paths to another processor", and identifies the one another processor. (column 22, lines 52-56) (Emphasis added). This is submitted to be unrelated to Applicants' invention of Claims 3, 12, 22 and 32, and, at best, the opposite of Applicants' invention.

For example, Claim 3 recites "upon said access testing by any of said plurality of testing processor nodes detecting a failure to access all of said other processor nodes, said failure detecting processor node posting a special identifier at said associated local error indicator."

Hence, Applicants respectfully submit that Claims 3, 12, 22 and 32 patentably define over Jardine under 35 U.S.C. 102(b), and respectfully request allowance thereover.

D) Claims 5, 14, 24 and 34:

The Examiner states that Jardine "discloses locking said posted identifier at said error indicator for a predetermined time-out period; and subsequent to expiration of said time-out period, deleting said posted identifier ***."

However, the claimed "posted identifier" of Claims 5, 14, 24 and 34, e.g. Claim 5, "said posted identifier", is the posted "identifier of said closest processor node having failed access at an associated error indicator local to said failure detecting processor node" of Claim 2.

Applicants respectfully submit that, as discussed above, Jardine is unable to determine the closest processor node, and has no interest in doing so, thereby teaching away from Applicants' invention. Applicants therefore respectfully submit that Applicants' Claims 5, 14, 24 and 34 patentably define over Jardine under 35 U.S.C. 102(b), and respectfully request allowance thereover.

E) Claims 6, 15, 25 and 35:

The Examiner states that Jardine "discloses locking said posted identifier at said error indicator; and responding to an operator initiated signal, deleting said posted identifier ***."

However, the claimed "posted identifier" of Claims 6, 15, 25 and 35, e.g., Claim 6, "said posted identifier", is the posted "identifier of said closest processor node having failed access at an associated error indicator local to said failure detecting processor node" of Claim 2.

Applicants respectfully submit that, as discussed above, Jardine is unable to determine the closest processor node, and has no interest in doing so, thereby teaching away from Applicants' invention. Applicants therefore respectfully submit that Applicants' Claims 6, 15, 25 and 35 patentably define over Jardine under 35 U.S.C. 102(b), and respectfully request allowance thereover.

F) Claims 7, 16, 26 and 36:

The Examiner states that Jardine "discloses locking said posted identifier at said associated local error indicator; and said displaying processor node retesting said access, and, upon absence of an error during a predetermined number of said retests, deleting said posted identifier ***."

However, the claimed "posted identifier" of Claims 7, 16, 26 and 36, e.g., Claim 7, "said posted identifier", is the posted "identifier of said closest processor node having failed access at an associated error indicator local to said failure detecting processor node" of Claim 2.

Applicants respectfully submit that, as discussed above, Jardine is unable to determine the closest processor node, and has no interest in doing so, thereby teaching away from Applicants' invention. Applicants therefore respectfully submit that Applicants' Claims 7, 16, 26 and 36 patentably define over Jardine under 35 U.S.C. 102(b), and respectfully request allowance thereover.

G) Claims 8, 17, 27 and 37:

The Examiner states that Jardine "discloses *** upon said access failure detecting step detecting access failure of a plurality of said multiple processor nodes at said single drop, said step of determining said processor node having failed access additionally comprises determining, from said relative locations, said single drop having failed access which is closest to said failure detecting processor node, ***."

As discussed above, Applicants respectfully submit that, without location or relative location information with respect to a multi-drop network, Jardine is unable to determine the "closest processor node" or the closest single drop, and has no interest in doing so, thereby teaching away from Applicants' invention. Therefore, Applicants' Claims 8, 17, 27 and 37 are submitted to patentably define over Jardine. For example, Claim 8 recites "upon said access failure detecting step detecting access failure of a plurality of said multiple processor nodes at said single drop, said step of determining said processor node having failed access additionally comprises determining, from said information of relative locations, said single drop having failed access which is closest to said failure detecting processor node, and selecting one of said multiple processor nodes at said single drop, said failure detecting processor node storing an identification of said selected processor node."

Applicants therefore respectfully submit that Applicants' Claims 8, 17, 27 and 36 patentably define over Jardine under 35 U.S.C. 102(b), and respectfully request allowance thereover.

H) Claims 9, 18, 28 and 38:

The Examiner states that Jardine "discloses one of said multiple processor nodes extending from said single drop of said multi-drop bus network is identified as having a higher priority than other processor nodes extending from said single drop, and wherein said selecting step comprises selecting said multiple processor node having said higher priority ***."

However, as pointed out by the accompanying Declaration under Rule 1.132, Jardine "describes monitoring communication among processors in a multi-path network, and which attempts to regroup in the event of a processor communication failure, e.g. 'an apparatus and protocol to determine the group of processors that will survive communications faults and/or timed-event failures in a multiprocessor system.' ***

"Jardine employs data structures, such as a matrix, that track the connectivity between the processors of the group in the multi-path network currently available to a processor." (Emphasis added).

Hence, Applicants respectfully submit that Jardine is unrelated to the multi-drop network of Claims 9, 18, 28 and 38 of Applicants, and sets no priorities since all of its processors of the Jardine network are connected by a multi-path network.

Thus, Applicants respectfully submit that Claims 9, 18, 28 and 38, e.g. Claim 9, "wherein one of said multiple processor nodes extending from said single drop of said multi-drop bus network is identified as having a higher priority than other processor nodes extending from said single drop, and wherein said selecting step comprises selecting said multiple processor node having said higher priority" patentably define over Jardine under 35 U.S.C. 102(b), and Applicants respectfully request allowance thereover.

I) Claims 19 and 29:

The Examiner states that Jardine "discloses wherein said local error indicators comprise character displays of at least one character ***".

However, Claims 19 and 29, e.g. Claim 19, "said local error indicators" refers to "a local error indicator *** posting, at said local error indicator associated with said failure detecting processor node, an identifier of said closest processor node having failed access." (Emphasis added).

Applicants respectfully submit that, as discussed above, Jardine is unable to determine the closest processor node, and has no interest in doing so, thereby teaching away from Applicants' invention. Applicants therefore respectfully submit that Applicants' Claims 19 and 29 patentably define over Jardine under 35 U.S.C. 102(b), and respectfully request allowance thereover.

**III) 35 U.S.C. 103, Claims 39-49:**

Claims 39-49 are rejected "under 35 U.S.C. 103(a) as being unpatentable over Jardine et al. in view of Rockwell (USPN 6,204,992).

A) Claim 39:

The Examiner rejects Claim 39 using similar language as with respect to Claims 1, 10, 20 and 30, and states "Jardine fails to explicitly state a robot accessor having a gripper and servo motors for accessing said data storage cartridges, said robot accessor having at least one processor node coupled to said

multi-drop bus network for operating said gripper and said servo motors in response to said linked commands.

"Rockwell discloses this limitation ***.

"Accordingly, it would have been obvious" to have the robot gripper "at least one processor node coupled to said multi-drop network ***".

However, Rockwell describes no multi-drop network, and describes no processor node for a robot accessor.

Rather, Rockwell describes a processor 24 for operating the actuator 26 and accessor 20. No other processor is coupled to processor 24 in any way. (See FIG. 2). The other processor in the figure is not coupled to processor 24, and, instead is separate and comprises "a data cartridge processor 14" (column 2, line 52), whose function is described as a separate entity at column 1, lines 15-16. Hence, Applicants respectfully submit that Rockwell also teaches away from Applicants' invention.

Hence, Applicants respectfully submit that, as with respect to Claims 1, 10, 20 and 30, without location or relative location information with respect to a multi-drop network, Jardine is unable to determine the "closest processor node", and has no interest in doing so, thereby teaching away from Applicants' invention. Rockwell is submitted also teach away from Applicants' invention. Therefore, Applicants' Claims 1, 10, 20 and 30 are submitted to patentably define over Jardine and Rockwell. Specifically, Claim 39 recites " a multi-drop bus network;

"at least one communication processor node for receiving commands, and coupled to said multi-drop bus network to provide a communication link for said commands;

"a robot accessor having a gripper and servo motors for accessing said data storage cartridges, said robot accessor having at least one processor node coupled to said multi-drop bus

network for operating said gripper and said servo motors in response to said linked commands;

"each of said processor nodes having information of relative locations of processor nodes on said multi-drop bus network; said processor nodes each independently testing access to other said processor nodes on said multi-drop bus network; upon said access testing by any of said testing processor nodes detecting a failure to access at least one of said other processor nodes, said failure detecting processor node determining, from said information of relative locations, the processor node having failed access which is closest to said failure detecting processor node; and said failure detecting processor node storing an identification of said closest processor node having failed access."

Therefore, Applicants respectfully submit that Applicants' Claim 39 patentably defines over Jardine and Rockwell under 35 U.S.C. 103(a), and respectfully request allowance thereover.

B) Claims 40-48:

Claims 40-48 are rejected based on Jardine and Rockwell under 35 U.S.C. 103(a) as above, and using language similar to that employed with Claims 2-9, 11-19, 21-29 and 31-38, above.

Accordingly, Applicants refer to the discussion with respect to Claims 2-9, 11-19, 21-29 and 31-38, above, together with the discussion with respect to Claim 39, above, and respectfully request allowance of Claims 40-48.

C) Claim 49:

The Examiner states that Jardine "fails to explicitly state additionally comprising a plurality of interconnected frames ***, at least one of said frames coupling said at least one robot processor node with said multi-drop bus network, at least one of said frames coupling said at least one communication processor node with said multi-drop network ***".

"Rockwell discloses this limitation ***. The additional racks *** are the additional interconnected frames discloses in claim 49.

"Thus, it would have been obvious ***" to have "at least one of said frames coupling said at least one robot access processor node with said multi-drop network, at least one of said frames coupling said at least one communication processor node with said multi-drop bus network ***".

However, as discussed above, neither Jardine nor Rockwell show or suggest a multi-drop network.

Further, Rockwell has only a single processor unconnected to any other processor.

Still further, neither Jardine nor Rockwell are able to determine the "closest processor node", and neither has interest in doing so, thereby teaching away from Applicants' invention. Therefore, Applicants' Claims 1, 10, 20 and 30 are submitted to patentably define over Jardine and Rockwell.

Specifically, Claim 49 recites "a plurality of interconnected frames, each having a plurality of said storage shelves, at least one of said frames coupling said at least one robot accessor processor node with said multi-drop bus network, at least one of said frames coupling said at least one communication processor node with said multi-drop bus network, said processor nodes in each of said frame comprising at least one said relative location."

Therefore, Applicants respectfully submit that Applicants' Claim 49 patentably defines over Jardine and Rockwell under 35 U.S.C. 103(a), and respectfully request allowance thereover.

**Additional Art:**

The additional references cited by the Examiner have been examined and as best understood, do not teach or suggest Applicants' claimed invention. The Examiner cited USPN 5,544,150, Fujimoto et al.; USPN 6,304,547, Tsuruta et al.; USPN 6,545,981, Garcia et al.; USPN 6,553,515, Gross et al.; USPN 6,606,299, Kurosawa et al.; USPN 6,625,751, Starovic et al.; USPN 6,665,811, de Azevedo et al.; USPN 6,690,648, Niida et al.; USPN 6,718,480, Ogura et al.; and USPA 2002/0191322, Jerman.

Applicants submit that none of the cited patents teach, either singly or in combination, the present invention as described and claimed in Applicants' Claims 1-49.

Accordingly, Applicants believe the present invention distinguishes over the cited patents and respectfully requests that the Examiner allow Applicants' Claims 1-49 under 35 U.S.C. 102 and 35 U.S.C. 103.

**SUMMARY:**

Applicants have amended typographical errors in Claims 2, 10 and 33, without the submission of new matter.

Applicants respectfully submit that the present invention distinguishes over the cited patents and respectfully requests that the Examiner allow Applicants' Claims 1-49 under 35 U.S.C. 102 and 35 U.S.C. 103.

Respectfully submitted,
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Attachment: Declaration under Rule 1.132